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10/540,066	06/22/2005	Shuji Hagino	1176/301	2635
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LIU & LIU 444 S. FLOWER STREET, SUITE 1750 LOS ANGELES, CA 90071			EXAMINER ALMEIDA, CORY A	
			ART UNIT	PAPER NUMBER
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/540,066	<b>Applicant(s)</b> HAGINO ET AL.	
	<b>Examiner</b> CORY A. ALMEIDA	<b>Art Unit</b> 2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 24 June 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-24 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 June 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)            | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | Paper No(s)/Mail Date. _____                                      |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## **DETAILED ACTION**

### ***Claim Objections***

1. Claim 12 and 23 is objected to because of the following informalities: claim 12 reads " said plurality of gray scale voltages and dose not select a second gray scale" and it should read "does" and not "dose". Appropriate correction is required.

### ***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 11-13, and 21-24 recite the limitation "third selecting means" in paragraph 2. There is insufficient antecedent basis for this limitation in the claim as there is no second selecting means.
4. Claims 19 and 20, recite the limitation "said predetermined ideal gray scale voltage" in paragraph 2 and "said series of outputting data" in paragraph 5. There is insufficient antecedent basis for these limitation in the claim as there is no second selecting means.

### ***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-6, 14-18 and 25-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Liu & Liu as disclosed in Applicants IDS.

7. In regards to claim 1, Liu and Liu disclose a gray scale voltage outputting device for outputting gray scale voltages in response to an image signal having a plurality of image data (Fig. 1, Data Input), wherein said device comprises a first selecting means (Fig. 1, 7) having a plurality of first inputting portions for receiving a plurality of gray scale voltage groups each of which has a plurality of gray scale voltages for selecting one of said received plurality of gray scale voltage groups (Fig. 1, 6), and wherein said device outputs one or more gray scale voltages of said plurality of gray scale voltages of said selected gray scale voltage group (Page 1, Par. 1).

8. In regards to claim 2, Liu and Liu disclose wherein said device comprises a first outputting means having a plurality of first outputting portions (Fig. 1, 6) for outputting said plurality of gray scale voltage groups to said plurality of first inputting portions of said first selecting means during a first predetermined period (Page 1, Par. 1).

9. In regards to claim 3, Liu and Liu disclose wherein said first outputting means comprises a generating means for generating said plurality of gray scale voltage groups (Fig. 1, 6), and wherein said generated plurality of gray scale voltage groups are outputted from said plurality of first outputting portions of said first outputting means during said first predetermined period (Page 1, Par. 1).

10. In regards to claim 4, Liu and Liu disclose wherein said image data is represented by a plurality of bits (Fig. 1, Data Input), and wherein the total number of said gray scale voltages of said generated plurality of gray scale voltage groups (Fig. 1,

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6) is equal to the number of bit patterns (Fig. 1, each line of Data Input) which said plurality of bits can take (Fig. 1).

11. In regards to claim 5, Liu and Liu disclose wherein said first selecting means selects one of said received plurality of gray scale voltage groups on the basis of a bit pattern of higher order bits of said plurality of bits (Page 2), said higher order bits comprising at least the most significant bit of said plurality of bits, and wherein said device outputs one or more gray scale voltages of said plurality of gray scale voltages of said selected gray scale voltage group on the basis of a bit pattern of lower order bits of said plurality of bits, said lower order bits comprising at least the least significant bit of said plurality of bits (Page 2).

12. In regards to claim 6, Liu and Liu disclose wherein said image data is represented by a plurality of bits (Fig. 1, Data Input), and wherein the total number of said gray scale voltages of said plurality of gray scale voltage groups (Fig. 1, 6) is smaller than the number of bit patterns which said plurality of bits can take (Page 1, Par. 1).

13. In regards to claim 14, Liu and Liu disclose wherein said first predetermined period comprises a first sub-period and a second sub-period, said first sub-period being for outputting a gray scale voltage corresponding to said image data having the least significant bit of a first logic, said second sub-period being for outputting a gray scale voltage corresponding to said image data having the least significant bit of a second logic (Fig. 2).

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14. In regards to claim 15, Liu and Liu disclose wherein said first sub-period precedes said second sub-period, and wherein said first sub-period is longer than said second sub-period (Fig. 2).

15. In regards to claim 16, Liu and Liu disclose wherein a first gray scale voltage group of said plurality of gray scale voltage group comprises a smaller gray scale voltage than a predetermined ideal gray scale voltage during a first frame period of successive frame periods, wherein a second gray scale voltage group of said plurality of gray scale voltage group comprises a higher gray scale voltage than said predetermined ideal gray scale voltage during a second frame period of said successive frame periods, wherein said first selecting means selects said first gray scale voltage group during said first frame period and selects said second gray scale voltage group during said second frame period, and wherein said device outputs said smaller gray scale voltage if said first selecting means selects said first gray scale voltage group and outputs said higher gray scale voltage if said first selecting means selects said second gray scale voltage group (Page 2).

16. In regards to claim 17, Liu and Liu disclose wherein said device comprises a processing means for processing a series of image data each of which having a predetermined bit pattern, wherein said processing means outputs said series of image data as a series of outputting data comprising a first outputting data and a second outputting data, said first outputting data having said predetermined bit pattern and said second outputting data having a different bit pattern from said predetermined bit pattern, and wherein said device outputs said smaller gray scale voltage during said first frame

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period and outputs said higher gray scale voltage during said second frame period on the basis of said series of outputting data (Fig. 2, Page 2).

17. In regards to claim 18, Liu and Liu disclose wherein said first selecting means selects one of said first and second gray scale voltage groups on the basis of a bit pattern of higher order bits of a first plurality of bits and selects the other of said first and second gray scale voltage groups on the basis of a bit pattern of higher order bits of a second plurality of bits, said first plurality of bits representing said first outputting data, said second plurality of bits representing said second outputting data (Page 2).

18. In regards to claim 25, Liu and Liu disclose wherein said first predetermined period comprises a first sub-period and a second sub-period, said first sub-period being for outputting a gray scale voltage corresponding to said image data having the least significant bit of a first logic, said second sub-period being for outputting a gray scale voltage corresponding to said image data having the least significant bit of a second logic (Fig. 2, Page 2).

19. In regards to claim 26, Liu and Liu disclose wherein said first sub-period precedes said second sub-period, and wherein said first sub-period is longer than said second sub-period (Fig. 2).

20. In regards to claim 27, Liu and Liu disclose an image display device comprising a gray scale voltage outputting device as claimed in claim 1 (Page 1, Par. 1).

***Claim Rejections - 35 USC § 103***

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

22. Claims 7-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu and Liu in view of Nitta, US-5774106.

23. In regards to claim 7, Liu and Liu does not disclose expressly wherein said first outputting means comprises a second selecting means, having a plurality of second inputting portions for receiving a plurality of reference voltage group each of which has a plurality of reference voltages, for selecting two of said received plurality of reference voltage groups, and wherein said first outputting means outputs said plurality of gray scale voltage groups from said plurality of first outputting portions on the basis of said selected two reference voltage groups.

Nitta discloses two selecting means receiving reference voltages and outputting gray scale voltages based on the two selection means (Fig. 22, Col. 12, 16-37).

At the time of the invention it would have been obvious to one of ordinary skill in the art to use the dual selection method of Nitta in conjunction with Liu and Liu.

The motivation for doing so would have been to generate more accurate gray scale voltages.



Therefore, it would have been obvious to combine Nitta with Liu and Liu to obtain the invention specified in claim 7.

24. In regards to claim 8, Nitta discloses wherein said second selecting means selects said two reference voltage groups on the basis of a bit pattern of higher order bits of said plurality of bits, said higher order bits comprising at least the most significant bit of said plurality of bits, wherein said first selecting means selects one of said received plurality of gray scale voltage groups on the basis of a bit pattern of intermediate order bits of said plurality of bits, and wherein said device outputs one or more gray scale voltages of said plurality of gray scale voltages of said selected gray scale voltage group on the basis of a bit pattern of lower order bits of said plurality of bits, said lower order bits comprising at least the least significant bit of said plurality of bits (Fig. 22, Col. 12, 16 – Col. 13, 4).

25. In regards to claim 9, Nitta discloses wherein at least one of said reference voltage groups is used as said gray scale voltage group (Fig. 22, Col. 12, 16 – Col. 13, 4).

26. In regards to claim 10, Nitta discloses wherein said first outputting means comprises a second outputting means having a plurality of second outputting portions for outputting said plurality of reference voltage groups to said plurality of second inputting portions of said second selecting means during a second predetermined period (Fig. 22, Col. 12, 16 – Col. 13, 4).

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27. In regards to claim 11, Liu and Liu does not disclose expressly said device comprises a third selecting means for selecting one or more gray scale voltages of said plurality of gray scale voltages of said selected gray scale voltage group.

Nitta discloses two selecting means receiving reference voltages and outputting gray scale voltages based on the two selection means (Fig. 22, Col. 12, 16-37).

At the time of the invention it would have been obvious to one of ordinary skill in the art to use the dual selection method of Nitta in conjunction with Liu and Liu.

The motivation for doing so would have been to generate more accurate gray scale voltages.

Therefore, it would have been obvious to combine Nitta with Liu and Liu to obtain the invention specified in claim 11.

28. In regards to claim 12, Nitta discloses wherein said first selecting means sequentially outputs said plurality of gray scale voltages of said selected gray scale voltage group to said third selecting means, and wherein said third selecting means selects a first gray scale voltage of said plurality of gray scale voltages and does not select a second gray scale voltage of said plurality of gray scale voltages, said first gray scale voltage corresponding to said bit pattern of said lower order bits and said second gray scale voltage being outputted from said first selecting means after said first gray scale voltage (Fig. 22, Col. 12, 16 – Col. 13, 4).

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29. In regards to claim 13, Nitta discloses wherein said third selecting means also selects a third gray scale voltage of said plurality of gray scale voltages, said third gray scale voltage being outputted from said first selecting means before said selected first gray scale voltage (Fig. 22, Col. 12, 16 – Col. 13, 4).

30. Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu and Liu in view of Nishio JP-08234697 as disclosed in IDS.

31. In regards to claim 19, Liu and Liu does not disclose expressly a third gray scale voltage group of said plurality of gray scale voltage groups comprises a predetermined gray scale voltage deviating from said predetermined ideal gray scale voltage, wherein said device comprises an additional voltage outputting means for outputting an additional gray scale voltage deviating from said predetermined ideal gray scale voltage, wherein one of said predetermined gray scale voltage and said additional gray scale voltage is larger than said predetermined ideal gray scale voltage and the other is smaller than said predetermined ideal gray scale voltage, and wherein said device outputs said predetermined gray scale voltage during one of said first and second frame periods and outputs said additional gray scale voltage during the other of said first and second frame periods on the basis of said series of outputting data..

Nishio discloses a third voltage group reference voltage  $V_{ref}$  which is output during the frame periods (Abstract).

At the time of the invention it would have been obvious to one of ordinary skill in the art to use the  $V_{ref}$  of Nishio in conjunction with Liu and Liu.

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The motivation for doing so would have been to generate more accurate gray scale voltages.

Therefore, it would have been obvious to combine Nishio with Liu and Liu to obtain the invention specified in claim 19.

32. In regards to claim 20 Nishio discloses, wherein said predetermined gray scale voltage is maximum gray scale voltage or minimum gray scale voltage (Abstract, Fig. 3).

33. Claims 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu and Liu in view of Nitta, US-5774106.

34. In regards to claim 21, Liu and Liu does not disclose expressly said device comprises a third selecting means for selecting one or more gray scale voltages of said plurality of gray scale voltages of said selected gray scale voltage group.

Nitta discloses two selecting means receiving reference voltages and outputting gray scale voltages based on the two selection means (Fig. 22, Col. 12, 16-37).

At the time of the invention it would have been obvious to one of ordinary skill in the art to use the dual selection method of Nitta in conjunction with Liu and Liu.

The motivation for doing so would have been to generate more accurate gray scale voltages.

Therefore, it would have been obvious to combine Nitta with Liu and Liu to obtain the invention specified in claim 21.

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35. In regards to claim 22, Nitta discloses wherein said device comprises a connection switching means for switching whether said third selecting means should be connected to said first selecting means or connected to said additional voltage outputting means (Fig. 22, 2210).

36. In regards to claim 23, Nitta discloses wherein said first selecting means sequentially outputs said plurality of gray scale voltages of said selected gray scale voltage group to said third selecting means, and wherein said third selecting means selects first gray scale voltage of said plurality of gray scale voltages and does not select a second gray scale voltage of said plurality of gray scale voltages, said first gray scale voltage corresponding to said bit pattern of said lower order bits and said second gray scale voltage being outputted from said first selecting means after said first gray scale voltage (Fig. 22, Col. 12, 16 – Col. 13, 4).

37. Claims 7-13 and 21-23 rejected under 35 U.S.C. 103(a) as being unpatentable over Liu and Liu in view of Nitta, US-5774106 in further view of Okada, US- 5923312.

38. In regards to claim 24 Nitta and Liu and Liu do not disclose expressly said third selecting means also selects a third gray scale voltage of said plurality of gray scale voltages, said third gray scale voltage being outputted from said first selecting means before said selected first gray scale voltage.

Okada discloses driving grey scale using 3 reference voltages (Fig. 25, Col. 8, 29-36 and Col. 17, 59 – Col. 18, 12).

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At the time of the invention it would have been obvious to a person of ordinary skill in the art to drive the gray scales of the combination of Nitta and Liu and Liu with three reference voltages of Okada.

The motivation for doing so would have been for uniform interpolation (Col. 18, 5-12).

Therefore, it would have been obvious to combine Okada with Nitta and Liu and Liu to obtain the invention as specified in claim 24.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CORY A. ALMEIDA whose telephone number is (571) 270-3143. The examiner can normally be reached on Monday through Friday 8AM to 4PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alexander Eisen can be reached on 571-272-7687. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CA

9/24/2008

/Alexander Eisen/  
Supervisory Patent Examiner, Art Unit 2629